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AN10352

-TDA9910HW- 12-bit High Speed A/D Converter Demonstration board

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Document information

Info	Content
Keywords	AN10352, TDA9910HW/6, TDA9910HW/8, Demoboard, 12-bit ADC, High speed, Application Note
Abstract	This document describes the design and the main features of the TDA9910 demonstration board (PCB1337-1) and how to use them. It includes the schematic files of the board.

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Revision history

Rev	Date	Description
01	20050701	First release

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1. Introduction

This application note describes the way to use the **TDA9910** demonstration board. The full schematic and printed layers are available on request.

The **TDA9910** is a 12-bit Analog-to-Digital Converter (ADC) optimized for direct IF sampling, and supporting the most demanding use conditions in ultra high IF radio transceivers for cellular infrastructure and other applications such as wireless access system, optical networking and fixed telecommunication. Thanks to its broadband input capabilities, the **TDA9910** is ideal for single and multiple carriers data conversion.

Operating at a maximum sampling rate of 80 Msample/s, analog input signals are converted into 12-bit binary coded digital words. All static digital inputs are CMOS compatible. All output signals are LVCMOS compatible. The **TDA9910** offers a flexible acquisition control system thanks to its programmable Complete Conversion Signal (CCS) that allows to adjust the delay of the acquisition clock used by the digital processing IC connected to TDA9910.

Thanks to its internal front-end buffer, the **TDA9910** offers the lowest input capacitance (< 1 pF) and therefore the highest flexibility in front-end anti-aliasing filter strategy.

The **TDA9910** is released in HTQFP48 package of which a representation is given on Figure 1:

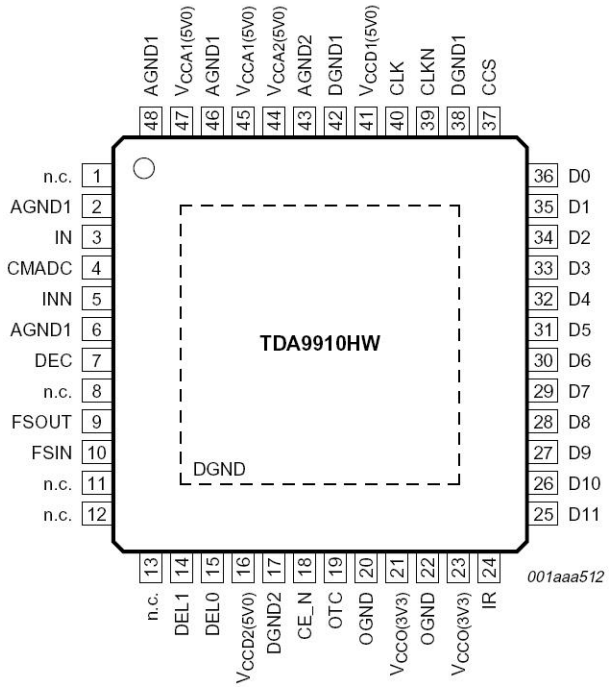


Fig 1. HTQFP48 package

2. Main features of the TDA9910HW

The **TDA9910HW** is a 12-bit Analog-to-Digital Converter. It can convert a typical analog input signal into 12 bits binary digital words at a maximum sampling rate of 80 Msps with a typical power dissipation of 870 mW.

The **TDA9910HW** codes the binary or the two's complement digital words on 3.3V CMOS digital outputs. On Figure 2 the block diagram is shown and the main specifications points are:

- Clock frequency: 60 / 80 Msps.
- Outputs voltage: 3.3 V.
- Power dissipation (typical): 870 mW.
- Accuracy: 12-bit.
- Supply: 5 V with output stages at 3.3 V.
- Compatibility: input: CMOS, output: TTL and CMOS (3.3 V).

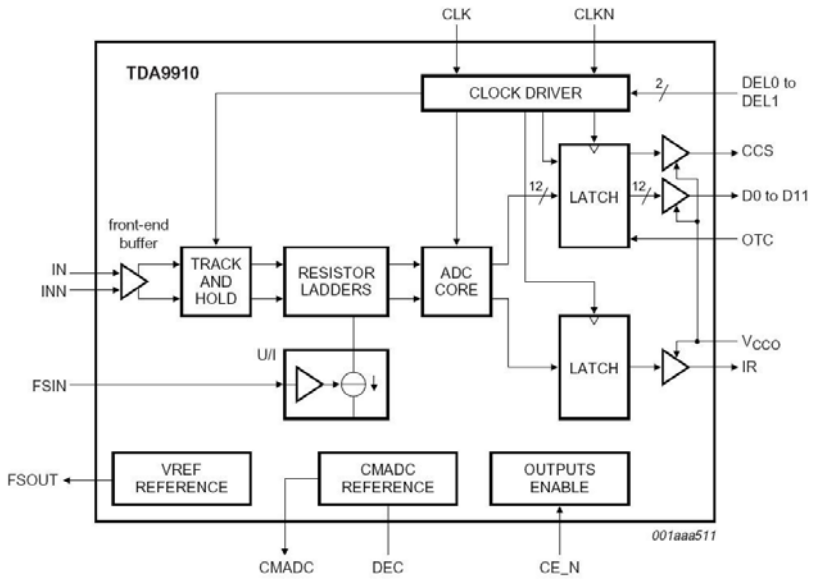


Fig 2. TDA9910 block diagram

3. Principle and description of the board

The principle of the Demonstration Board for the **TDA9910**, which is described in this Application Note, is shown on Figure 3:

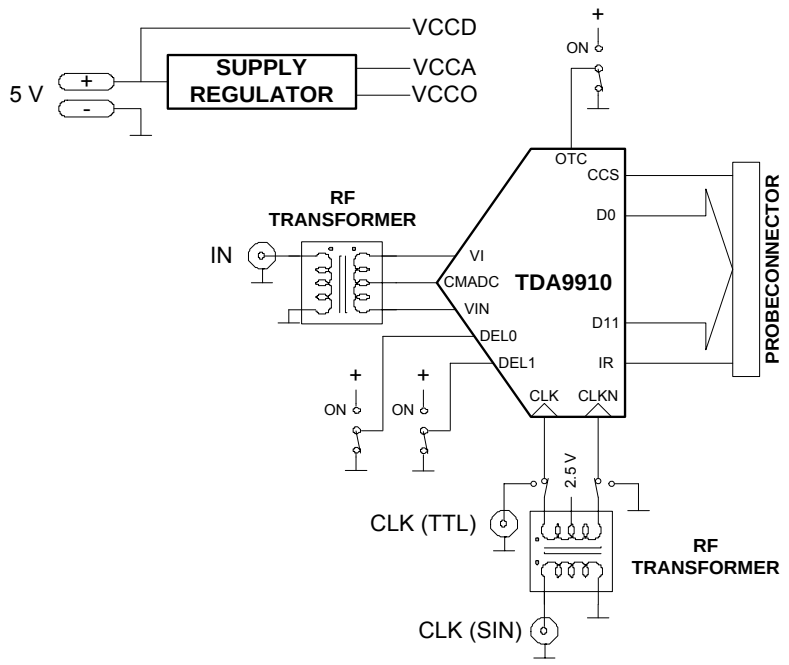


Fig 3. Functional block diagram of the demoboard

The different functions of the demoboard are:

1. **TDA9910HW**: **A**nalog-to-**D**igital **C**onverter converting an analog signal into 12 bits binary digital words.
2. **Power supply regulator**: The demoboard works with a single +5 V_{DC} external power supply. The right supply plugging is indicated by a green LED.
3. **Input stage**: A RF transformer transforms the single analog signal applied on the board into a symmetrical differential analog signal on the ADC analog inputs. The input common mode and the full scale control bias voltages are provided by the TDA9910 (CMADC and FSOUT).
4. **Clock stage**: A TTL / CMOS clock signal is advised to drive the converter but a RF transformer allows the use of a sine wave clock signal.
5. **Control inputs**: Three switches allow to control the CCS delay and the output coding. The chip enable function is fixed to active.
6. **Output stage**: A probe connector is used to connect the data to a logic analyser.

4. Overview of the board

The whole implantation of the **TDA9910HW** demoboard is shown on Figure 4:

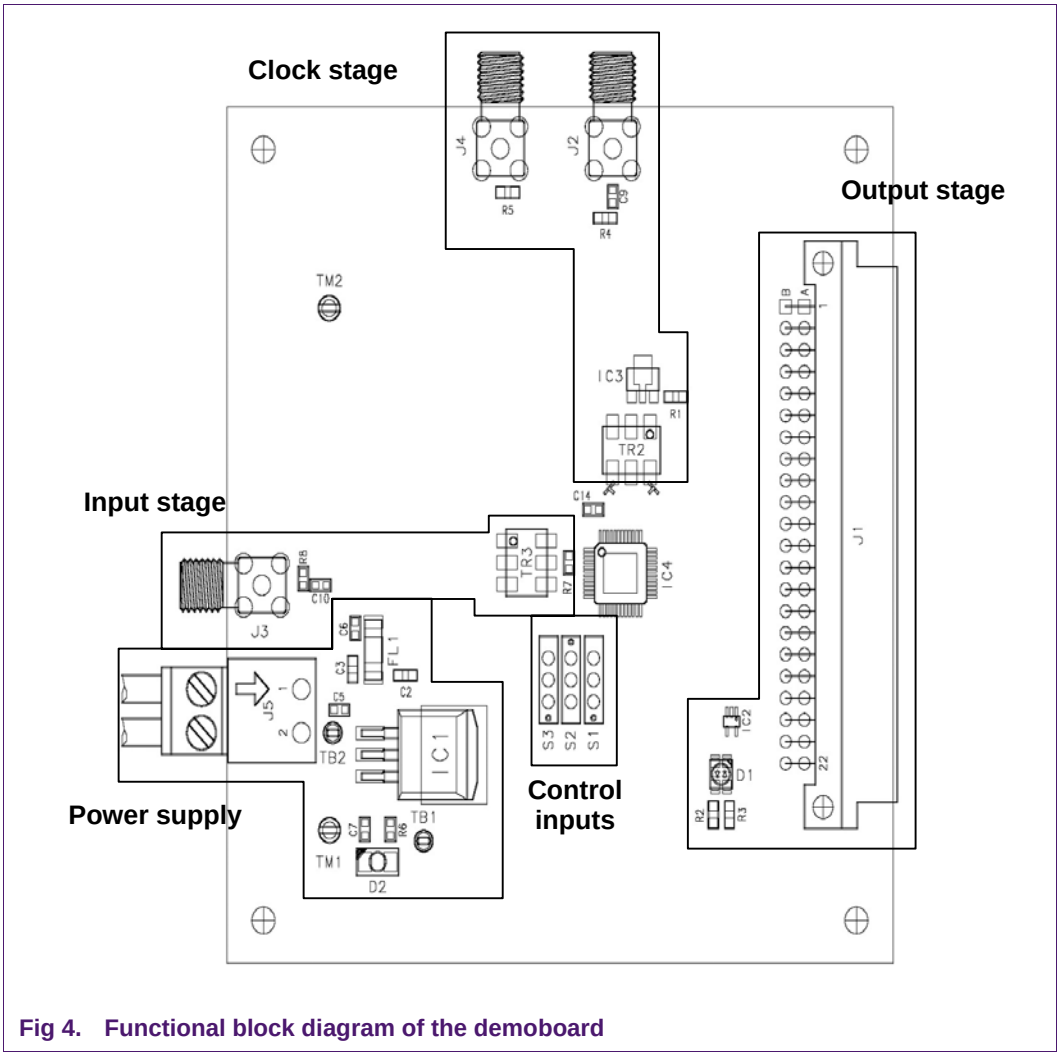


Fig 4. Functional block diagram of the demoboard

The different connectors, potentiometers, switches, lights and test-points available on the board are:

1. TDA9910HW
   - **IC4**, TDA9910 device in a HTQFP48 package.
2. Power supply regulator
   - **J5**, a two-points PHOENIX connector connected to an external +5 V power supply.
   - **TB1**, test-point to control the V_{CCO} supply voltage (+3.3 V).
   - **TB2**, test-point to control the V_{CCD} and V_{CCA} supply voltages (+5 V). It is connected to the external power supply.

- **D2**, a green light to indicate the right supply plugging.

3. Input stage
   - **J3**, a SMA connector with 50 Ω equivalent impedance for the analog input signal (IN).
4. Clock stage
   - **J4**, a SMA connector with 50 Ω for the ADC external TTL / CMOS clock input (CLK TTL).
   - **J2**, a SMA connector with 50 Ω for the ADC external sine wave clock input (CLK SIN).
5. Control inputs
   - **S1**, a switch to choose the ADC two's complement outputs (OTC).
   - **S2**, **S3**, two switches to enable the complete conversion output signal (CCS) and to add a delay between this signal and the ADC digital outputs D0 to D11.
6. Output stage:
   - **J4**, a probe array connector corresponding to the ADC digital outputs (D0 to D11), the complete conversion signal (CCS) and the out of range of the analog input signal **(**IR) is available to connect the logic analyser that acquires the data.
   - **D1**, an IR bicolor light to indicate the in (green) or out (red) of range of the analog input signal applied.

5. PCB design

The design is made on a multi-layer Printed Circuit Board. The technological concept used to make this PCB is given on Figure 5:

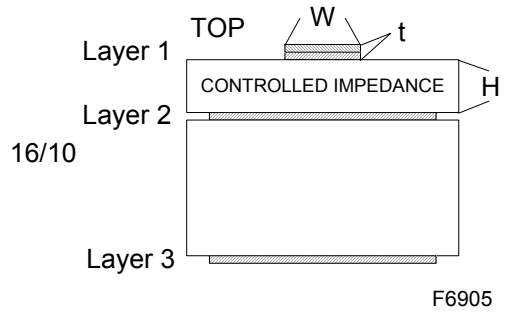


Fig 5. PCB structure

Three physical copper layers are used. The first layer (Cu layer with SnPb layer) is the signal layer which contains the microstrip lines. The second layer (Cu layer) is made of the ground planes corresponding to the signal layer. The third layer is designed especially for the power supply wires.

The metallic hole technique is used to make all the necessary interconnections between the layers. The dielectric substrate is an Epoxy Glass resin with a relative permittivity (ε_r) of 4.7 and a first layer thickness (t) of 47µm (≈ 1.8 mils). The substrate thickness (H) is 178 µm (≈7mils) between the first and the second layer.

To calculate the width (**W**) of the 50 Ω matched lines (analog input and clock signals), the Kaup's relation was used:

$$W = \frac{5.98H}{0.8e^{\frac{Zo\sqrt{\varepsilon_r + 1.41}}{87}}} - \frac{t}{0.8},$$

(Accurate to within 5% when $0.1 < \frac{W}{H} < 3.0$ and $1 < \varepsilon_r < 15$).

hence:

W ≈ 285.8 µm (≈ 11 mils),

where:

- Zo = 50 Ω
- t = 47 µm (≈ 1.8 mils)
- H = 178 µm (≈ 7 mils)
- ε_r = 4.7

6. Special features of the demoboard

6.1 Binary and two's complement output coding

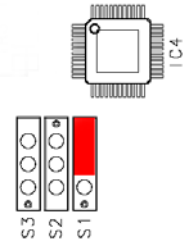
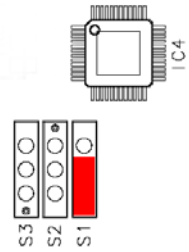
The switch **S1** corresponding to the two's complement input **OTC** allows the choice of either the *binary* or the *two's complement* digital words as shown in Table 1:

Table 1: Binary/two's complement output coding

Step	IR	*Binary* outputs bits D11 to D0	*Two's complement* output bits D11 to D0
underflow	0	000000000000	100000000000
0	1	000000000000	100000000000
1	1	000000000001	100000000001
.	.	.	.
2047	1	011111111111	111111111111
.	.	.	.
4094	1	111111111110	011111111110
4095	1	111111111111	011111111111
overflow	0	111111111111	011111111111

The *binary* mode is enabled when the switch **S1** is on **BIN**, the *two's complement* mode is enabled when the switch **S1** is on **TWO**. In the Table 2 is given the relationship between the different choices:

Table 2: Selection mode

OTC	D11 to D0	Switches
BIN	binary	
TWO	two's complement	

6.2 Clock generation

On the demoboard, the clock connectors **J2** and **J4** allow to drive the ADC clock input according to Table 3:

Table 3: Logic families and AC signal

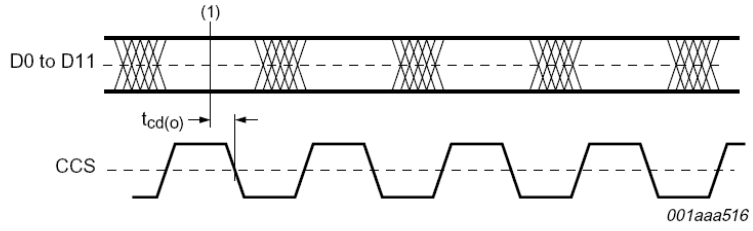
Logic family	J4 CLK (TTL)	J2 CLK (SIN)
TTL/CMOS	TTL/CMOS	-
AC	-	1.5 $V_{p-p\ (typ)}$

The selection between one clock or the other is made with the straps at the RF transformer output. To use the TTL/CMOS clock, connect the CLK input pin to CLK(TTL) connector and the CLKN input pin to the ground. To use the sine-wave clock, connect the CLK and CLKN input pins to the RF transformer.

6.3 Complete conversion signal CCS

The complete conversion signal **CCS** pin is directly connected to the probe array connector **J4**.

The switches **S2** and **S3** corresponding to complete conversion delay **DEL0** and **DEL1** allow either to disable the complete conversion signal **CCS** output signal or to add a delay between this **CCS** signal and the output data **D0** to **D11**. The timing diagram is shown on Figure 6:

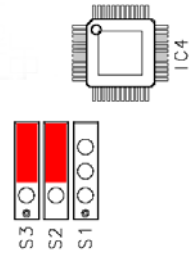
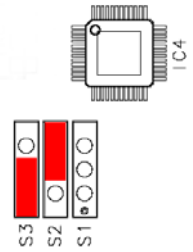
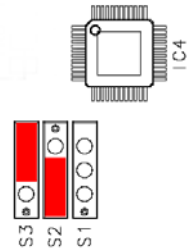
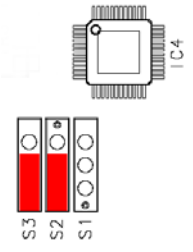


(1) $t_{cd(o)}$ is referenced to the middle of the active data.

Fig 6. CCS timing diagram

On the Table 4 are given the relationship between the different states:

Table 4: Complete conversion signal states and delays

DEL1	DEL0	CCS	t_{cd}	Switches
0	0	high impedance	-	
1	0		0.2 ns	
0	1	active	1.3 ns	
1	1		2.4 ns	

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